REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove.

Claims 1-22 are pending. Claims 1-4, 6-17, and 19-21 are rejected and Claims 5, 11, 18, and 22 are objected to. Claims 9, 11, 21, and 22 are amended hereinabove.

Regarding the drawing objection, the Applicant is unable to submit annotated sheets showing "changes made to the previous version" because there were no changes between the original drawing set and the replacement formal drawing set. The replacement formal drawing set was prepared by the Assignee's professional outside patent drafting firm and electronically filed with the USPTO on July 28, 2006 because the original drawing set was prepared with an automated drawing program and is of inferior quality.

Independent Claim 1 positively recites a column of asymmetric memory cells spanning opposing bit lines in alternating orientations. These advantageously claimed features are not taught or suggested by the patent granted to Naiki or the APA; either alone or in combination.

The Applicant respectfully traverses the statements in the Office Action (page 3) that Naiki teaches asymmetric memory cells in alternating orientations. The Applicant submits that the term "asymmetric memory cell" is defined in the Specification as having a fast side and a slow side (paragraph 0024; see also paragraphs 0006 and 0025). Furthermore, the term "alternating orientations" is defined in the Specification as the fast sides and slow sides of the memory cells being connected to the bit-line or bit-line-bar in an alternating fashion (paragraphs 0026-0028, FIG. 1). Naiki does not teach the advantageously claimed invention because Naiki does not teach asymmetric memory cells in alternating orientations. Instead, Naiki teaches the physical displacement of memory cells within the surface of a semiconductor wafer (column 2 lines 15-21; column 5 lines 10-15, 18-22, and 48-58; FIG. 9). Similarly, the APA does not teach the advantageously claimed invention because the APA does not teach asymmetric memory cells in alternating orientations (paragraph 0005). Therefore, the combination of Naiki and the APA also does not teach asymmetric memory cells in alternating orientations, as advantageously claimed.

Regarding Claim 8, the Applicant respectfully traverses the statement in the Office Action (page 5) that Naiki discloses an SRAM device having first and second opposing orientations. The Applicant submits that Naiki teaches that all

cells in a column are of the same orientation (i.e. an all even row or an all odd row; column 6 lines 42-45 and 55-67; FIG. 9).

For the reasons stated above, the Applicant respectfully traverses the Examiner's rejection of Claim 1 and respectfully asserts that Claim 1 is patentable over the patent granted to Naiki and the APA; either alone or in combination. Furthermore, Claims 2-8 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

Independent Claim 9 positively recites a column of asymmetric SRAM cells spanning opposing bit lines in alternating orientations. These advantageously claimed features are not taught or suggested by the patent granted to Naiki or the APA; either alone or in combination.

The Applicant respectfully traverses the statements in the Office Action (pages 5 and 7) that Naiki teaches asymmetric memory cells in alternating orientations. The Applicant submits that the term "asymmetric memory cell" is defined in the Specification as having a fast side and a slow side (paragraph 0024; see also paragraphs 0006 and 0025). Furthermore, the term "alternating orientations" is defined in the Specification as the fast sides and slow sides of the memory cells being connected to the bit-line or bit-line-bar in an alternating

fashion (paragraphs 0026-0028, FIG. 1). Naiki does not teach the advantageously claimed invention because Naiki does not teach asymmetric memory cells in alternating orientations. Instead, Naiki teaches the physical displacement of memory cells within the surface of a semiconductor wafer (column 2 lines 15-21; column 5 lines 10-15, 18-22, and 48-58; FIG. 9). Similarly, the APA does not teach the advantageously claimed invention because the APA does not teach asymmetric memory cells in alternating orientations (paragraph 0005). Therefore, the combination of Naiki and the APA also does not teach a column of asymmetric SRAM cells spanning opposing bit lines in alternating orientations, as advantageously claimed.

The Applicant notes that Naiki teaches that the spanning cells are all in the same direction for a given pair of opposing bit lines (column 6 lines 62-68; column 7 lines 1-6, 33-39, and 44-55). The voltage signals are applied to the implied sensing circuitry according to the pair of selected bit lines (i.e. the even column or the odd column).

For the reasons stated above, the Applicant respectfully traverses the Examiner's rejection of Claim 9 and respectfully asserts that Claim 9 is patentable over the patent granted to Naiki and the APA; either alone or in combination. Furthermore, Claims 10-13 are allowable for depending on allowable

independent Claim 9 and, in combination, including limitations not taught or described in the references of record.

Independent Claim 14 positively recites configuring a column of asymmetric memory cells to span opposing bit lines in alternating orientations. These advantageously claimed features are not taught or suggested by the patent granted to Naiki or the APA; either alone or in combination.

The Applicant respectfully traverses the assertion in the Office Action (page 5) that Naiki teaches configuring a column of asymmetric memory cells to span opposing bit lines in alternating orientations. The Applicant submits that the term "asymmetric memory cell" is defined in the Specification as having a fast side and a slow side (paragraph 0024; see also paragraphs 0006 and 0025). Furthermore, the term "alternating orientations" is defined in the Specification as the fast sides and slow sides of the memory cells being connected to the bit-line or bit-line-bar in an alternating fashion (paragraphs 0026-0028, FIG. 1). Naiki does not teach the advantageously claimed invention because Naiki does not teach configuring a column of asymmetric memory cells to span opposing bit lines in alternating orientations. Instead, Naiki teaches the physical displacement of memory cells within the surface of a semiconductor wafer (column 2 lines 15-21; column 5 lines 10-15, 18-22, and 48-58; FIG. 9). Similarly, the APA does not teach the advantageously claimed invention because the APA does not teach

configuring a column of asymmetric memory cells to span opposing bit lines in alternating orientations (paragraph 0005). Therefore, the combination of Naiki and the APA also does not teach configuring a column of asymmetric memory cells to span opposing bit lines in alternating orientations, as advantageously claimed.

For the reasons stated above, the Applicant respectfully traverses the Examiner's rejection of Claim 14 and respectfully asserts that Claim 14 is patentable over the patent granted to Naiki and the APA; either alone or in combination. Furthermore, Claims 15-20 are allowable for depending on allowable independent Claim 14 and, in combination, including limitations not taught or described in the references of record.

Independent Claim 21 positively recites a first SRAM cell having a first pass gate connected to the first bit line and a second pass gate wider than the first pass gate connected to the second bit line, and also a second SRAM cell having a first pass gate connected to the second bit line and a second pass gate wider than the first pass gate connected to the first bit line. These advantageously claimed features are not taught or suggested by the patents granted to Najm et al. or Yamauchi; either alone or in combination.

Najm et al. does not teach the advantageously claimed invention because Najm et al. does not teach a first SRAM cell having a first pass gate connected to the first bit line and a second pass gate wider than the first pass gate connected to the second bit line, and also a second SRAM cell having a first pass gate connected to the second bit line and a second pass gate wider than the first pass gate connected to the first bit line (paragraph 0034, FIG. 2). Similarly, Yamauchi does not teach the advantageously claimed invention because Yamauchi does not teach a first SRAM cell having a first pass gate connected to the first bit line and a second pass gate wider than the first pass gate connected to the second bit line, and also a second SRAM cell having a first pass gate connected to the second bit line and a second pass gate wider than the first pass gate connected to the first bit line (column 4 lines 13-45; FIGS. 1-3). Therefore, the combination of Najm et al. and Yamauchi also does not teach a first SRAM cell having a first pass gate connected to the first bit line and a second pass gate wider than the first pass gate connected to the second bit line, and also a second SRAM cell having a first pass gate connected to the second bit line and a second pass gate wider than the first pass gate connected to the first bit line, as advantageously claimed.

For the reasons stated above, the Applicant respectfully traverses the Examiner's rejection of Claim 21 and respectfully asserts that Claim 21 is patentable over the patents granted to Najm et al. and Yamauchi; either alone or

in combination. Furthermore, Claim 22 is allowable for depending on allowable independent Claim 21 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

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